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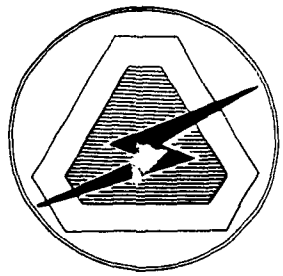
USAELRDL Technical Report 2333

BULK RELIABILITY EFFECTS IN SEMICONDUCTOR DEVICES

CURRENT CROWDING IN TRANSISTORS

Bernard Reich

Edward B. Hakim



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UNITED STATES ARMY
ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, N.J.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
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BULK RELIABILITY EFFECTS IN SEMICONDUCTOR DEVICES; CURRENT CROWDING IN TRANSISTORS

Bernard Reich

Edward B. Hakim

DA TASK NR. 3A99-21-002-01

ABSTRACT

The problem of current crowding in transistors is reviewed and its relationship to transistor performance described. A method is described whereby a quantitative value can be assigned as a measure of the extent of crowding that occurs. The possible implications of current crowding in the operational reliability are described. An empirical figure of merit is developed relating the crowding factor to the physical parameters of the semiconductor device. Recommendations in device design are made which should improve the current handling capability of transistors.

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BULK RELIABILITY EFFECTS IN SEMICONDUCTOR DEVICES; CURRENT CROWDING IN TRANSISTORS

INTRODUCTION

An effect which has existed in junction transistors since their inception has been that of current crowding. For the purposes of this report current crowding is defined as a condition, due to high current densities, whereby device characteristics or performance which is dependent on current density may be altered. This effect has been considered by others[1,2] in the past, possibly from a somewhat different viewpoint. Yet, based on a group of planar epitaxial transistors examined at this Laboratory, much variation exists in these devices from the point of view of their crowding characteristic. It appears that the reason for the crowding is due to the effect outlined by Fletcher,[2] i.e., emitter electrode cut-off due to transverse base biasing. From the technical and advertising literature published on the more recent structure, it appears that the primary emphasis has been placed on emitter geometry in an attempt to reduce the effects of current crowding. From the study conducted at this Laboratory, it appears that there are other factors that are currently being overlooked which may be of equal or greater importance than the design of the emitter area and periphery.

DISCUSSION

The Effects of Current Crowding in Transistors

Current crowding exhibits itself in many different ways with respect to the parametric and functional characteristics of transistors. The first, which may be noted by anyone examining transistor characteristics, is the severe fall-off of common emitter current gain at high current levels. It is interesting to note that in most transistor types this variation in current gain with bias current is different from manufacturer to manufacturer. This is evident in the simpler structures, such as the alloy junction transistor, extending to and including the more advanced planar epitaxial devices. As a result, there is a lesser or greater degree of fall-off of dc, low frequency, and high frequency current gain with increasing bias current. Furthermore, the performance of devices in the functional transmission and switching applications is directly affected by this fall-off of current gain.

In addition, there have been indications from other work performed that current crowding and the phenomena of secondary breakdown are related.[3] When current crowding occurs, the effective area of emission may be reduced causing the creation of hot spots at the emitter periphery and resulting in thermal runaway.

Finally, there have been indications from work done under Army Materiel Command sponsorship that current crowding may affect the operational life of devices. It has been observed that during power step-stressing, with current accounting for the change in power, the log-normal curve

obtained by plotting failures versus stress temperature may be altered. If current crowding is not accounted for, then the extrapolations made, based on a combination of power and temperature stresses, might be in error. This is illustrated in Fig. 1 where a log-normal plot is made of the variation of failure rate as a function of inverse absolute temperature. The data combine both storage and operational step-stress figures on a single curve. From measurements made, it was known that this device exhibited current crowding at the current levels where the power step-stress tests were performed. Therefore, the curve obtained from the power points had a steeper slope than the curve obtained from the temperature points. An extrapolation of the power curve alone would result in lower assumed failure rates at the normal operating points.

There have been recommendations made with respect to the above problem, some of which seem to conflict. Fletcher[2] suggests that the base width of the transistor be reduced as much as possible, consistent with other design considerations of the device. Another theory, with respect to the solution of the secondary breakdown problem,[4] suggests that a widening of the base width alleviates the problem. If it is assumed that both the secondary breakdown and the current crowding problem are related, then the solutions are conflicting.

A suggested solution to the problem of current crowding has been that of increasing the ratio of emitter periphery to emitter area. As a result of this proposal, a variety of emitter designs have been promulgated to accomplish this end, as can be noticed in the advertising literature of many companies. While it is felt that this consideration is of importance, there appear to be factors in the device design which if overlooked could negate the gains obtained through the emitter geometrical design.

The Measurement of Current Crowding and Its Relationship to Transistor Characteristics

In this discussion, it is important to be able to quantitatively assign some value to current crowding primarily for comparison purposes. Techniques have been established at this Laboratory which indicate the extent of crowding and the current at which the action commences. The first method utilized to measure crowding was the variation of thermal resistance, θ, as a function of collector or emitter current. In this method of measurement (following a procedure developed at this Laboratory[5]), current gain is the temperature sensitive parameter and the measurement is made on a continuous basis. If a plot is made of θ versus I_E or I_C, it is observed that there is a rise in θ at high current levels as shown in Fig.2. In Fig. 2 the solid portion of the curve represents the actual data points and the dashed portion represents extrapolated points. The degree of crowding is measured by the slope of the curve of Fig. 2. The equation expressing this curve after the onset of crowding is given by:

$$\theta = \theta_o \exp kI \qquad (1)$$

where

θ_o is the thermal resistance extrapolated to zero collector current; $^oC/W$

k is the slope of the line

and

I is the collector current in amperes.

The factor, "k", in Eq.(1) is the crowding factor. Values of "k" noted during the course of this study for various device types are shown in Table I. In this table, the smaller the value of the factor, "k", the greater the current the device will handle prior to the commencement of crowding. From many observations, it has been found that the reciprocal of "k" is approximately the current at which crowding begins. For example, if we choose the NPN Si Triple Diffused Device from Table I, its "k" factor is 2.8. From this the current crowding begins at 1/2.8 amperes or approximately 360 ma. Within any given category of device, such as with the Ge Alloy PNP power transistor, or any similar grouping, variations of 2:1 in the values of "k" are not uncommon.

From the data listed in Table I, it appears that area alone is not the only governing factor related to current crowding. Si planar epitaxial device #1, having an emitter area of seven square mils, has a "k" factor which is much lower than the units having much larger area, i.e., units #2 and #3.

The question may now be raised as to what significance the factor, "k", bears to transistor performance. In Fig. 3 a plot is made of the variation of thermal resistance with current in addition to the variation of the low frequency current gain, h_{fe}. The unit used for the characteristic shown in Fig. 2 is the same device that yields the characteristic of Fig.3. It is interesting to note that the rise in thermal resistance above 0.2 amperes and the fall-off of current gain h_{fe} are both exponential. Furthermore, the positive slope of the thermal resistance curve is, for all practical purposes, equal to the negative slope of the h_{fe} characteristic; the value of the slope for the thermal resistance curve being +2.9 and for the h_{fe} curve -3.0. While data has been presented to illustrate this point for one device, similar correlation between the rise in thermal resistance and the fall-off in current gain has been noted for units made by other manufacturers and for other manufacturing processes. From the above data and observations, it appears that the fall-off of small signal low frequency current gain h_{fe}, as a function of collector current at high injection levels, can be expressed as:

$$\frac{h_{fe1}}{h_{fe2}} = \exp -k\ (I_2 - I_1) \qquad (2)$$

where

h_{fe1} is the small signal current gain at the lower current level, I_1, (amperes)

h_{fe2} is the small signal current gain at the higher current level, I_2, (amperes)

and k is the slope of the h_{fe} vs I_C curve.

Of particular interest is the fact that while the factor, "k", appears in both the expressionsfor the modified value of thermal resistance at the fall-off of current gain, their values are obtained differently. Although the thermal resistance technique employs current gain as the temperature

sensitive parameter, it depends on the variation of h_{fe} with temperature to accomplish the measurement. It is assumed that in the small signal gain versus collector current measurement, the gain is independent of temperature. Yet under these two conditions, θ vs I_C and h_{fe} vs I_C, the values of "k" noted are the same.

Determination of the Device Parameters Affecting Current Crowding

If it is assumed that current crowding is responsible for the rise in thermal resistance and the fall-off of current gain at high injection levels, then the conclusions reached by Fletcher[2] should apply to the observations noted in this study. The work by Fletcher was based entirely on alloy transistors. However, the assumptions used in the derivation of equation (3) will also be valid for diffused devices.

The assumptions used are:

"1. The conductivity of the emitter region is very large so that emitter efficiency approaches unity.

2. The conductivity of the base region is sufficiently high that it is not severely deterred by the presence of injected carriers at the levels considered.

3. Flow of minority carriers across the base region is by field-aided diffusion, the effective diffusion coefficients being g times the normal coefficient where $1 \leqq g \leqq 2$.

4. Recombination of injected holes in the base region is approximately monomolecular and described by an effective lifetime τ which is independent of injected carrier concentration in range considered."

As well as these assumptions, the idealized case of a "semi-infinite one-dimensional transistor" was used.

Based on the above hypothesis, Fletcher[2] derives an expression for the variation of current density as a function of distance from the base lead connection which is given by:

$$j(x) = j_{(o)} \left[1 + x \sqrt{\frac{\rho}{4} \frac{q}{kT} \frac{W}{D_p \tau_p} j_{(o)}} \right]^{-2} \qquad (3)$$

where

x is the distance from the base contact
ρ is the base resistivity
W is the base width
and $j_{(o)}$ is the current density assuming the absence of crowding.

If the characteristic frequency f_T is expressed as a time constant,

$$T_{ec} = \frac{1}{2\pi f_T}$$

then, f_T can be computed by the evaluation of the components of its associated time constant:

$$T_{ec} = T_e + T_b + \frac{T_x}{2} + T_c$$

$$\text{then, } f_T = \frac{1}{2\pi\left[T_e + T_b + \frac{T_x}{2} + T_c\right]} \qquad (8)$$

where;

$T_e = C_e r_e \qquad r_e = kT/qI_E$

$T_b = T_a + T_d$

$T_a = \frac{1}{W_\alpha}$ and T_d = time constant associated with excess phase

$\frac{T_x}{2}$ = collector depletion-layer transit time

T_c = time constant associated with collector series resistance.

It is now assumed that due to the planar epitaxial structure and in the frequency and current range under consideration, $T_c + T_x \ll T_e + T_b$ and equation (8) reduces to:

$$f_T \approx \frac{1}{2\pi\left[T_e + T_b\right]} . \qquad (9)$$

Since T_b is independent of I_E, it is possible to separate the time constances associated with f_T by determining f_T at different emitter currents.

Equation (9) can then be rewritten as:

$$\frac{1}{f_T} \approx \frac{1}{f_{T_e}} + \frac{1}{f_{T_b}} . \qquad (10)$$

It has been shown[9] that,

$$f_\alpha \approx f_b = \left[\frac{W^2}{nD_p}\right]^{-1} \text{ where, } 2 \leq n \leq 6 \qquad (11)$$

$$\text{therefore, } \frac{1}{f_T} \approx \frac{1}{f_{C_e r_e}} + \frac{1}{f_\alpha} . \qquad (12)$$

From Eq. (3), therefore, for any given geometry it is important to keep the term:

$$x \sqrt{\rho/4 \; \frac{q}{kT} \; \frac{W}{D_p \; \tau_p} \; j(o)} \qquad (4)$$

as small as possible with respect to unity in order to reduce current crowding. From Fletcher's study one conclusion was reached concerning the design of more efficient emitters, along with several other conclusions based on term (4) above. Since that time much effort has been placed on obtaining emitters with large ratios of peripheral length to overall emitter area.

From the examination of the data on several different silicon planar transistors, some of which are shown in Table I, it became apparent that the above term could be further reduced by optimizing other device design parameters. In particular, four different types of silicon planar epitaxial transistors were examined for current crowding. The devices, all specified as switching transistors, were examined to determine the current at which crowding began by using the θ vs I_C characteristic. Furthermore, particular attention was directed to two parameters, ρ and W of term (4), and their relationship to the maximum current density prior to the onset of crowding.

In order to measure, ρ, the base resistivity, the emitter to base capacitance was measured at various reverse bias levels below the emitter base breakdown voltage. During these measurements, the collector-to-base diode was not biased. Following the capacitance measurements, the capacitance vs voltage curve was extrapolated back to zero voltage and a value of capacitance designated as "C_o" obtained. Since the transistors had graded emitter-base junctions, it has been shown[6] that the barrier capacitance per area is equal to:

$$C = \frac{K\epsilon_o}{2} \left[\frac{2q \; (N_d - N_a)}{3K\epsilon_o V'} \right]^{1/3} . \qquad (5)$$

It is then assumed that:

$$C_o \approx A_e \; (\; \sigma_b \;)^{1/3} \qquad (6)$$

thus

$$\sigma_b \approx (C_o/A_e)^3 \qquad (7)$$

where C_o is the capacitance at zero emitter voltage ($\mu\mu f$)

A_e is the area of the emitter junction ($mils^2$)

σ_b is the conductivity of the base region.

In order to obtain an indication of the base width of these devices, a measurement of f_T was made, based on the following reasoning.[7,8]

The terms derived from the above calculations were used to determine a figure of merit which was felt related to term (4). This relationship was based on the premise that the only terms in expression (4) which varied with voltage and or current were W and ρ . Thus. from equation (7), $\sigma_b \approx \left(\frac{C_o}{A}\right)^3$ and from (11). $W \approx \left(f_\alpha\right)^{-\frac{1}{2}}$; f_α could then be determined by measuring f_T ; equation (12). For the planar epitaxial devices examined, the easily measured parameters above were used as the figure of merit;

$$F.M. = \left(\frac{C_o}{A_e}\right)^3 \left(f_\alpha\right)^{-1}/2 .$$

The above figure of merit was then compared to the maximum current density at which the device could operate before crowding occurred. This information was obtained from examination of the characteristic of Fig. 1 and knowing the geometrical area. The results obtained are shown in Table II.

From Table II, it is worth noting that the current at which crowding began was below the specified maximum value in three of four cases. Furthermore, the greater the value of the FM, the greater the current density prior to current crowding. Also to be noted is the large variation in the FM, indicating that if improvements were made to increase its value the greater performance could be obtained. The data shown in Table II was plotted in Fig.4 to illustrate graphically the role of the figure of merit with respect to maximum current handling capability prior to crowding. The data in Fig.4 and Table II indicate that the greater the doping level under the emitter and the narrower the base width, the greater the FM, hence improved current handling capability. The authors believe that the curve of Fig.4 can be used to predict the current at which crowding begins for any other silicon planar device if the FM is known.

It is felt that the data presented above is in agreement with Fletcher's original predictions as to the design factors leading to the reduction of current gain fall-off with increasing bias current. Yet, from the devices examined, the resistivity and base width considerations may not have been given the necessary attention for device improvement.

CONCLUSIONS

From this study it has been concluded that:

(1) Current crowding occurs in most devices, usually below the maximum specified current rating, and could possibly degrade device performance within its ratings. By the use of a curve derived in this report from a plot of current density vs a figure of merit, the current at which crowding begins can be determined.

(2) A figure of merit has been developed for silicon planar epitaxial devices which is felt is in agreement with Fletcher's[2] results. However, much can be done to improve the current gain linearity with current. The most significant device parameter which could be altered is base

conductivity. Nevertheless, it appears that altering this parameter might conflict with many electrical specification requirements on base emitter breakdown voltage as well as effects due to decreased life time. If a relaxation of this electrical parameter could be tolerated, then improved devices could be designed with superior gain-linearity characteristics with bias current. It appears that if the current handling range of this class of device is to be extended to the multi-ampere range the base resistivity will have to be reduced in accordance with the results noted in this report.

(3) Because current crowding results in increased thermal resistance, its effect must be taken into account during the operational life of the device. In addition, its presence must also be accounted for in step-stress testing where current is utilized as a stress. If crowding is ignored, then the possibility exists that a true acceleration factor might not be obtained.

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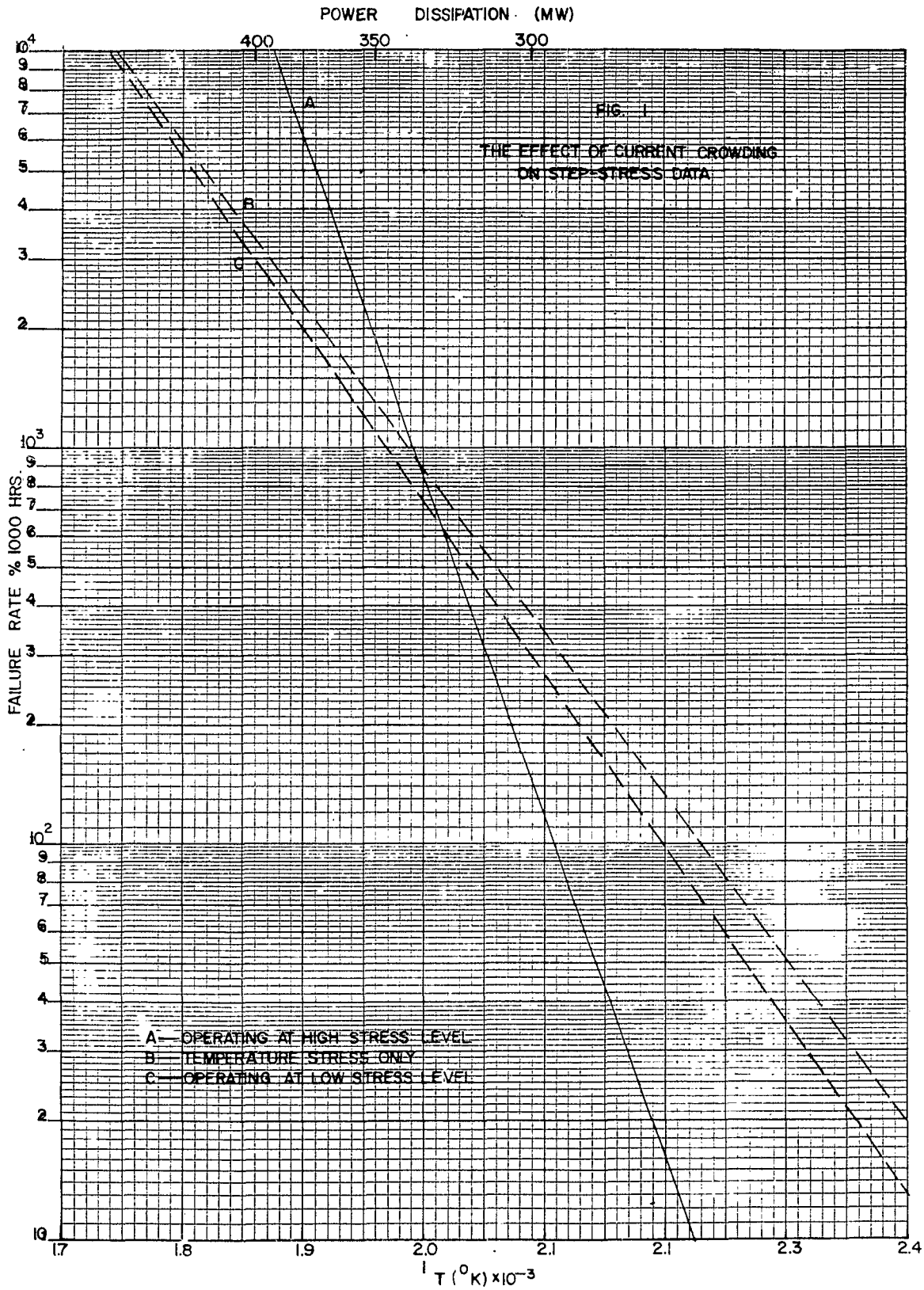

FIG. 1

THE EFFECT OF CURRENT CROWDING ON STEP-STRESS DATA

Fig 2

THERMAL RESISTANCE TO CASE VS. CURRENT Si PLANAR EPITAXIAL TRANSISTOR

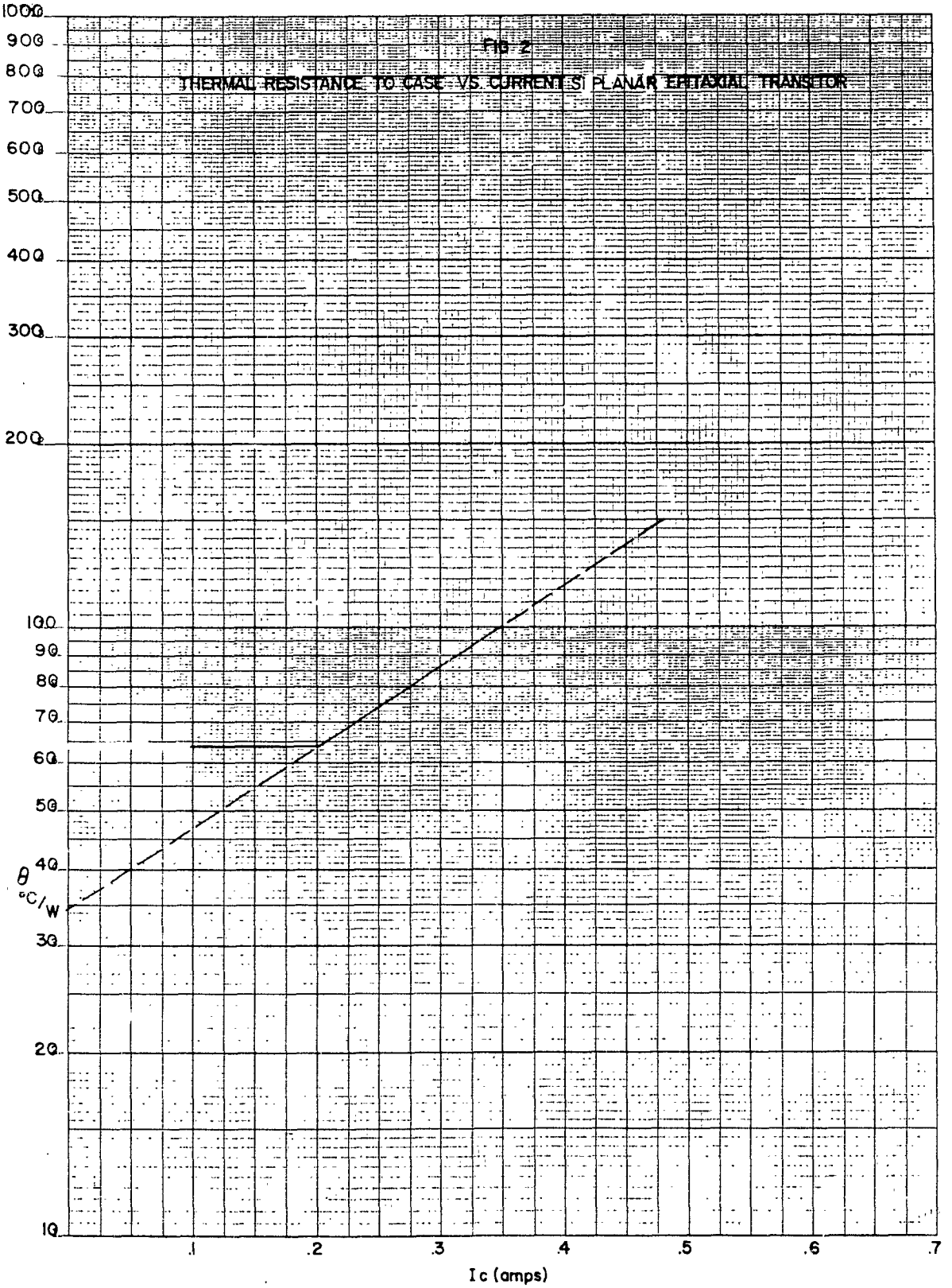

FIG.3

THERMAL RESISTANCE AND CURRENT GAIN
V.S. CURRENT Si PLANAR EPITAXIAL TRANSITOR

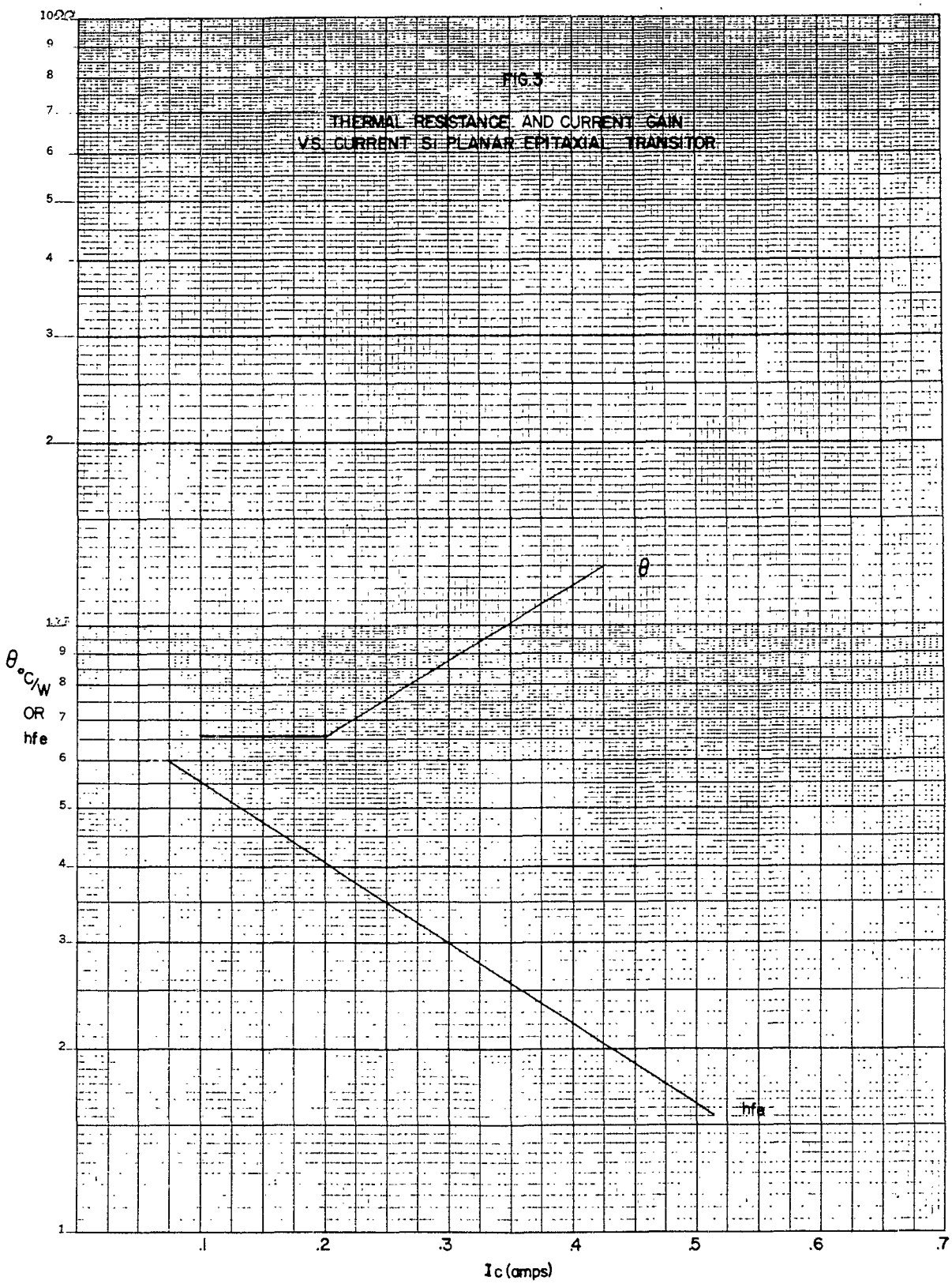

FIG 4

FIGURE OF MERIT V.S. MAXIMUM CURRENT DENSITY Si PLANAR EXPITAXIAL DEVICE

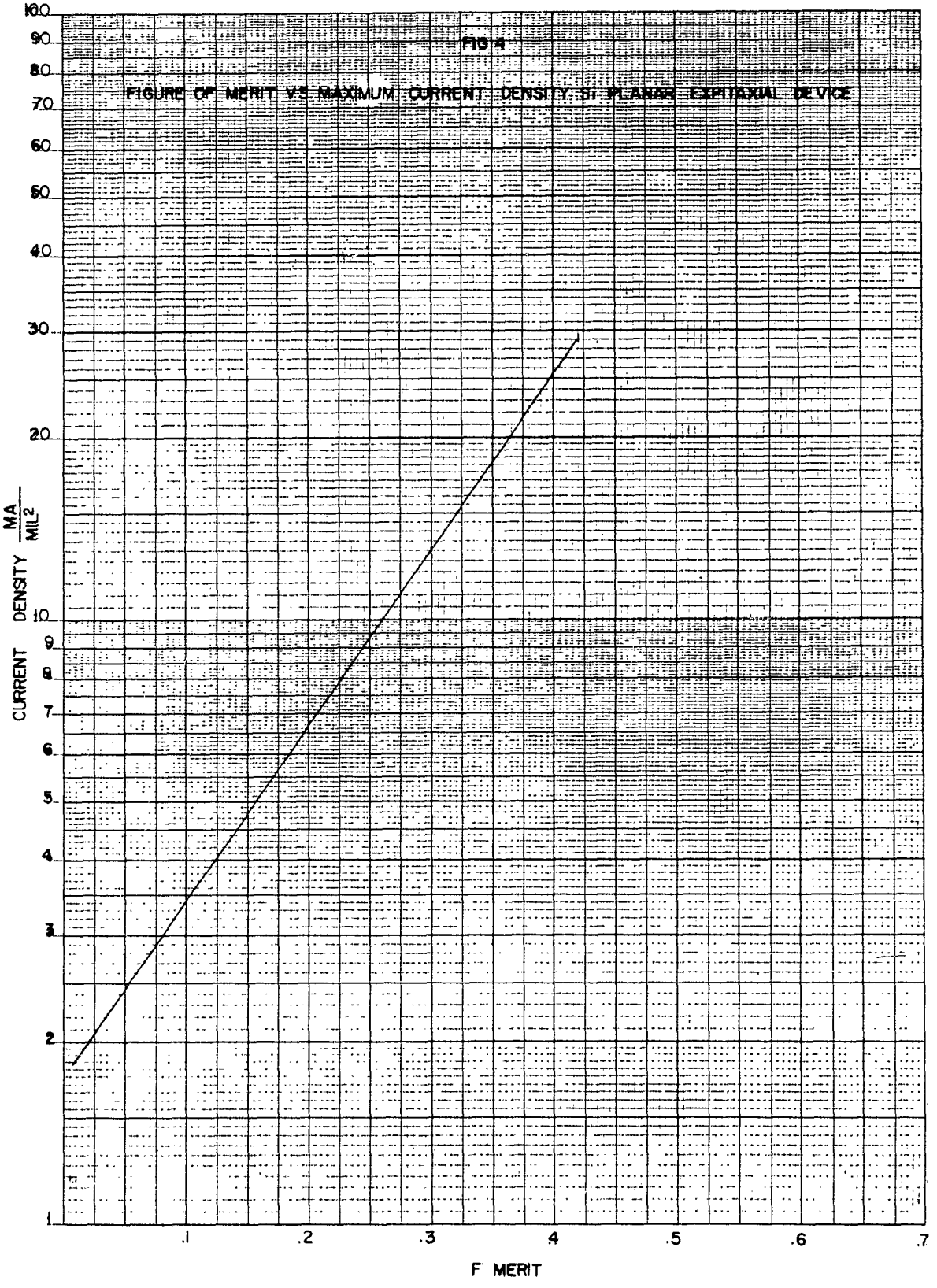

TABLE I

CROWDING FACTOR, k, FOR SEVERAL TRANSISTOR TYPES *

TRANSISTOR TYPE	EMITTER AREA MILS^2	"k" FACTOR
PNP Ge Alloy #1	12,000	0.26
PNP Ge Alloy #2	____	0.47
PNP Ge Alloy #3	____	0.51
NPN Si Planar Epitaxial #1	7	4.8
NPN Si Planar Epitaxial #2	16	16.3
NPN Si Planar Epitaxial #3	43	8.0
NPN Si Planar Epitaxial #4	176	2.8
NPN Si Planar Epitaxial #5	210	2.0
NPN Si Triple Diffused	____	2.8

* The numbers #1, #2, #3, etc. are indicative of devices from different manufacturers.

TABLE II

FIGURE OF MERIT VERSUS MAXIMUM CURRENT DENSITY
(Si planar epitaxial transistors)

Epitaxial Type	Emitter Area Mil^2	Mfrs. Specified Maximum Current MA	Current at which Crowding Began MA	FM $\left(\frac{C_o}{A}\right)^3 \left(f_\alpha\right)^{-1/2} \left(\frac{\mu\mu f}{mil^2}\right)^3 \left(\frac{Mc}{sec}\right)^{-1/2} x10^{-2}$	I/A $\frac{ma}{Mils^2}$
1	7	200	200	.42	29
2	16	200	120	.21	7.5
3	43	500	150	.08	3.5
4	176	1000	330	.015	1.85

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1. Transistors
2. Reliability
3. Transistor Design

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